CLAIMS

What is claimed is:

1. A system comprising:

a plurality of execution units, each of said execution units including one or more data registers and one or more shadow registers, each shadow register being communicatively coupled to at least one data register in another execution unit;

a memory unit; and

a control unit operable to issue control signals to the execution units, the control signals being operable to facilitate processing of data read from the memory unit, and to enable data transfers between the execution units.

2. A system as in claim 1, in which each shadow register is connected to an input to a data register, such that data written to the data register is also written to the shadow register.

3. A system as in claim 1, in which the plurality of execution units include one or more integer execution units and one or more datapath execution units.

4. A system as in claim 2, in which the data register comprises an accumulator register.

5. A system comprising:

a control unit;

a first execution unit, the first execution unit including a first data register; and

a second execution unit, the second execution unit including a second register containing a copy of the first data register's contents, the second register being communicatively coupled to an input of the first data register.

6. The system of claim 5, in which the first execution unit comprises a datapath execution unit.

7. The system of claim 5, in which the second execution unit comprises an integer execution unit.

8. The system of claim 6, in which the second execution unit comprises an integer execution unit.

9. The system of claim 7, in which the first execution unit comprises an integer execution unit.

10. The system of claim 5, in which the first data register comprises an accumulator register.

11. A system comprising:

a general purpose processor;

a memory unit;

a user interface; and

a plurality of special-purpose processors, at least one of the special purpose processors comprising:

a plurality of datapath units, each of said datapath units including a data register;

an integer unit, the integer unit including one or more shadow registers, each shadow registers being communicatively coupled to a data register in a datapath unit; and

a control unit operable to issue control signals to the integer unit and the datapath units.

12. The system of claim 11, in which the plurality of processors form part of a chip designed in accordance with a reconfigurable communications architecture.

13. A method comprising:

at a first execution unit, calculating a first result;

storing the first result in a first data register at the first execution unit; and

transferring the first result from the first execution unit to a first shadow register in a second execution unit.

14. The method of claim 13, in which the acts of storing the first result in the first data register and transferring the first result to a first shadow are performed during the same clock cycle.

15. The method of claim 13, further comprising:

at a third execution unit, calculating a second result;

storing the second result in a second data register at the third execution unit; and

transferring the second result from the third execution unit to a second shadow register in the second execution unit.

16. The method of claim 15, in which the act of transferring the first result from the first execution unit to the first shadow register is performed during the same clock cycle as the act of transferring the second result from the third execution unit to the second shadow register.

17. The method of claim 15, in which the act of transferring the first result from the first execution unit to the first shadow register is performed at a frequency independent of the act of transferring the second result from the third execution unit to the second shadow register.

18. The method of claim 13, further comprising:

at the second execution unit, calculating a second result;

storing the second result in a second data register at the second execution unit; and

transferring the second result from the second execution unit to a third shadow register in a third execution unit.

19. The method of claim 13, in which the first execution unit comprises a datapath execution unit and the second execution unit comprises an integer execution unit.

20. The method of claim 13, in which the second execution unit comprises an integer execution unit and the first execution unit comprises an integer execution unit.

21. The method of claim 13, in which the second execution unit comprises a datapath execution unit and the first execution unit comprises a datapath execution unit.